A METHOD AND APPARATUS FOR CONTROLLING THE HEAD VELOCITY OF A HARD DRIVE DURING RAMP LOAD/UNLOAD

FIELD OF THE INVENTION

The present invention relates to a method and apparatus for controlling the transducer head velocity of a disk drive during a ramp load or unload procedure. More particularly, the present invention provides for the control of the transducer heads using a microprocessor to determine the speed of the heads and, accordingly, to make velocity adjustments.

BACKGROUND OF THE INVENTION

A hard disk drive is a device with one or more disks, or platters, on which digital information is stored in the form of magnetic charges. The disks are mounted on and rotated by a cylindrical spindle assembly. Contemporary hard disk drives typically include an actuator, a rotary actuator structure that is powered by a voice coil motor ("VCM"), an actuator arm extending from the VCM, and a transducer head disposed at the end of the actuator arm. The rotary actuator structure positions one or more slider head assemblies at desired locations relative to surfaces of the magnetic disk or disks. A hard disk read/write head, which is used to read and write the data to and from the magnetic disk, is mounted onto the slider head assembly. Thus, the slider physically supports the head and holds it in the correct position relative to the hard disk platter as the head floats over the surface. While the actuator assembly is actuated by a VCM, a spindle motor rotates the magnetic disk or disks.

In modern disk drives the heads are generally parked, or stopped, at the inner diameter of the disk, such as a landing zone, whenever the

spindle assembly is at rest. A landing zone is an area of the disk that is designated as either a takeoff or landing spot for the heads while the spindle starts spinning or stops moving respectively. Once the spindle motor begins to accelerate, the read/write heads are dragged onto the disks until the disks accelerate to a speed at which the heads will fly, or separate, from the disk platter.

To minimize the friction between the read/write head and the hard disk, the surface of the disk is usually textured to create a "rough" surface. As the storage capacity of hard disk drives increases every year, the flying height of the read/write heads decreases. Thus, a hard disk surface must be very smooth to avoid damaging either the heads and/or the disk drive. If, for example, the heads are parked onto the smooth surface of the disk, the contact friction between the head and the disk increases dramatically. As a result, an increase in current may be required to break the head loose from the disk drive to allow the spindle to rotate, or spin up.

This concern is relevant today as manufacturers of modern disk drives are increasingly designing smaller form factors, or disk sizes, (2.5", 1.8" and 1" so far), particularly in battery-operated devices. An increase in the current required to rotate the spindle is therefore not desirable. Additionally, a smaller form factor reduces the disk surface area and the total disk data area, which is reduced further if a separate landing zone is employed. Finally, smaller form factor disk drives are more susceptible to operational and non-operational shock, which could be more damaging if the head and disk are in contact.

To overcome these constraints, disk drive manufacturers have implemented a ramp structure where the heads are lifted off the disk and are parked onto a separate ramp. In a ramp structure, the read/write heads do not fall to the surface of the disk when the disk's motor stops. Rather, the heads are lifted from the surface of the disk while the drive is still spinning and are parked onto special ramps. After the read/write

heads have ascended the ramp, the disks decelerate and stop spinning. When the power is reapplied to the spindle motor, the process is reversed. The disks spin up, and once the disks have accelerated to a speed such that the heads fly without contacting the disk surface, the heads are moved off the ramps and onto the surface of the disk platters.

During a ramp load/unload procedure, the velocity of the read/write head is accurately controlled to avoid damaging the head, or the disk at the point of contact, thereby compromising the disk drive reliability and quality. As the actuator coil moves through its magnetic poles, it generates a back emf voltage, ("V_{bemf}"), which is proportional to its speed. Thus, V_{bemf} is an indicator of the actuator velocity and therefore may be accurately measured to provide feedback of the head velocity. The V_{bemf} voltage may be calculated by first determining the overall voltage across the VCM coil. The total voltage across the VCM coil is: $V_{bemf} + I_{vcm}*R_{vcm}$. To measure the V_{bemf}, therefore, the term $I_{vcm}*R_{vcm}$, which represents the VCM "IR" drop, is removed from the equation, thereby isolating the V_{bemf} voltage.

There are two methods by which the V_{bemf} voltage may be isolated and measured. First, a Pulse Width Modulation technique may be used. Second, an IR cancellation technique may be employed. In the Pulse Width Modulation ("PWM") technique, the VCM is turned off periodically, forcing the current in the VCM coil, I_{vcm}, to go to zero. Thus, the "IR" drop across the VCM coil equals zero and the V_{bemf} voltage may be readily measured. In the IR cancellation technique the V_{bemf} voltage is determined by measuring the gain in a servo loop. Unlike the PWM technique, the current to the VCM is not periodically turned off in the IR cancellation technique. Rather, some calibrations may be required to cancel the IR component from the VCM voltage. Such calibrations may need to be repeated because temperature and voltage deviations may cause the gain of the servo loop to change frequently over time.

Of the two V_{bemf} measurement techniques discussed above, the PWM technique is easier to implement. The PWM technique requires less hardware and fewer calibrations than the IR cancellation technique. However, the load/unload process of the VCM in the PWM technique may be audible and therefore inappropriate for applications in which audible noise is not desirable. The IR cancellation, however, may itself not be appropriate for certain applications, as it is more sophisticated than the PWM technique and requires a robust calibration technique with more associated hardware. Further, an increase in the resolution of the voltage measurements may require a hardware design change because the resolution and accuracy of the measurements is a function of the number of bits of the A/D converter.

In the prior art, hardware had to be specifically designed for either the PWM or IR cancellation techniques. If both techniques were needed for a particular application, two distinct sets of hardware had to be implemented, possibly increasing the overall cost of the system. Further, during the implementation of the measurement techniques, a decision as to which technique would be employed needed to be made prior to any voltage measurements, thereby greatly reducing the system flexibility.

For the reasons stated above and for other reasons presented in greater detail in the detailed description of the present specification, there is a desire for a system that allows for the accurate control of a disk read/write head during a ramp load/unload procedure. In particular, there is a need for a system that may employ either a PWM technique or an IR calibration technique to measure the back emf voltage without the need for hardwiring a specific measurement technique or making multiple system calibrations prior to operation of the disk drive.

SUMMARY OF THE INVENTION

To achieve these and other advantages and in accordance with the purposes of the present invention, as embodied and broadly described, a

method and apparatus for controlling the velocity of a read/write disk head during a ramp load/unload are disclosed.

According to an embodiment of the present invention, a method for accurately measuring the V_{bemf} voltage using either of two different techniques; PWM and IR cancellation, and a means for making real-time adjustments to the velocity of the voice coil motor (VCM) is disclosed. The method includes measuring, amplifying, and transporting to a microprocessor the voltages across a voice coil motor (V_{motor}) and a sense resistor (V_{Rsense}). The method further includes calculating the V_{bemf} voltage of the VCM and making real-time adjustments to the VCM velocity.

According to another embodiment of the present invention, an apparatus to control the velocity of a transducer head during a ramp load/unload is disclosed. The control circuitry includes a driver circuit that powers the VCM, a multiplexer, an analog-to-digital converter (ADC), and a microprocessor. The microprocessor typically calculates the VCM velocity based on a measured V_{bemf} voltage.

BRIEF DESCRIPTION OF THE DRAWINGS

These and other advantages of the present invention are more fully described in the following drawings and accompanying text in which like reference numbers represent corresponding elements throughout:

FIG. 1 illustrates a cross-section of a hard disk drive assembly;

FIG. 2 illustrates a block diagram of the art ramp load/unload procedure;

FIG. 3 illustrates a schematic of the ramp load/unload control in accordance with a preferred embodiment of the present invention;

FIG. 4 illustrates a flowchart of a microprocessor calibration algorithm in accordance with the present invention; and

FIG. 5 illustrates a flowchart of a load/unload algorithm in accordance with the invention; and

FIG. 6 illustrates a flowchart of a velocity compensation algorithm in accordance with the present invention.

DETAILED DESCRIPTION

FIG. 1 depicts a prior-art hard disk drive 100. The prior-art hard disk drive 100 includes an actuator 110 having a voice coil motor (VCM), disks 120, or platters, a cover 130, an actuator arm 140, a spindle 150, read/write heads 160, a base casting 170, and sliders 180. A hard disk drive 100 uses round flat disks 120, or platters, that are coated on both sides with a special media material designed to store information. The disks 120 are mounted and stacked onto the cylindrical spindle 150 that, during operation, rotates the disks 120 at a high speed. Electromagnetic read/write heads 160 are mounted onto the sliders 180 and are used to record or read information to or from the disks 120. The sliders 180 are mounted onto actuator arms 140 that are connected mechanically into a single assembly and positioned over the surface of the disk 120. The sliders 180 and the actuator arms 140 move the read/write heads 160 as needed for read/write operations. The hard disk drive 100 is enclosed by a cover 130 and a base casting 170.

A ramp load/unload in the hard drive 200 is illustrated in FIG. 2. The hard drive 200 includes a ramp 210, a détente (rest) position 220, an actuator 110, an actuator arm 140, a disk 120, a slider 180, a read/write head 160, and a read/write position 240. During read/write operations, the read/write heads 160 fly over the surface of the disk 120, at the read/write position 240, as a result of an air cushion caused by the rotation of the disks 120. During the ramp unload, the actuator 110 moves the slider 180 and read/write head 160 onto the special ramp 210 while the disk 120 is still spinning.

The read/write head 160 comes to rest at the détente position 220, which is used by the hard disk drive 200 as a landing zone on the hard drive 200. After the read/write head 160 comes to rest onto the détente

position 220, the hard disk drive 200 stops the rotation of the disk 120. Similarly, during the ramp load, the hard disk drive 200 increases the rotation of the disk 120. When the disk 120 is spinning at a velocity where the read/write head 160 can fly above the disk 120 without making contact, the actuator 110 moves the slider 180 and read/write head 160 off the special ramp 210 and onto the disk 120.

In order to control the velocity of the slider and the read/write head 160 up and down the ramp 210, one embodiment of the present invention uses a ramp load/unload control circuitry 300. The control circuitry 300 includes a driver circuit 310 that powers the VCM, a multiplexer 370, an analog-to-digital converter (ADC) 380, and a microprocessor 390. The microprocessor 390 typically calculates the VCM velocity based on a measured V_{bemf} voltage 340. There are two methods by which the back emf voltage may be isolated and measured. First, the Pulse Width Modulation may be used. Second, the IR cancellation technique may be employed. In the Pulse Width Modulation ("PWM") technique, the VCM is turned off periodically, forcing the current in the VCM coil, I_{vcm}, to go to zero. Thus, the "IR" drop across the VCM coil equals zero and the bemf voltage, V_{bemf}, is readily measured. Unlike the PWM technique, the current to the VCM is not periodically turned off in the IR cancellation technique. Rather, some calibrations may be required to cancel the IR component from the VCM voltage. Such calibrations may need to be repeated because temperature and voltage deviations may cause the gain of the servo loop to change frequently over time. After it calculates the V_{bemf} voltage, the microprocessor 390 performs a control loop compensation before controlling the input to the driver circuitry 310. The output of a driver circuit 310 is connected to both a resistance of the voice coil motor, R_{vcm}, 320 and the positive input of a first operational amplifier 350.

When the read/write heads 160 are moved across the magnetic disk, the back emf voltage, V_{bemf} 340, opposes the motion of the heads 160. As

the velocity of actuator arm 140 increases, the magnitude of V_{bemf} increases. To measure this voltage, an external sense resistor, Rsense 330 may be placed in series with V_{bemf} 340 and R_{vcm}, 320. Rsense 330 may then be connected to the negative input of the first operational amplifier 350 and to the positive input of a second operational amplifier 360. The other side of Rsense 330 may be connected to the negative input of the second operational amplifier 360 and to an output of the driver circuit 310.

The output of the first operational amplifier 350 and the output of the second operational amplifier 360 are coupled to a multiplexer 370. The operational amplifiers 350 and 360 output signals are referenced to a Reference voltage, Vref 357. An analog-to-digital converter (ADC) 380 converts the multiplexed analog signals into a digital format before they are received by microprocessor 390. The microprocessor 390 calculates the VCM velocity, as described below in Figure 4, does the desired control loop compensation, and sends the appropriate control signal to the input of the driver circuit 310.

When the disk drive is initialized at power-up, the driver circuit 310 is off and the current to the VCM, I_{vcm}, is zero. At this point, the transducer heads are stationary, and the back emf voltage, V_{bemf} 340, is 0. The microprocessor 390 receives a voltage level from the first operational amplifier 350, Vvcm 353, which is equal to Vref 357, and designates the voltage as Vref1. The microprocessor 390 then receives a voltage level from the second operational amplifier 360, which is equal to Vref 357, and designates it as Vref2. To determine the exact offset in each path, Vref is measured through the paths of Vvcm 353 and the sense resistor, V_{Rsense}.

The microprocessor 390 then determines the output level in both paths of Vvcm 353 and V_{Rsense} 355 for the ADC 380 voltage corresponding to no current flowing in the VCM coils. The microprocessor 390 calibrates the control circuitry 300 using the calibration algorithm 400 described

below. This method of calibration calculates the gain coefficient, Kcal, using the following IR cancellation technique:

Kcal may be defined as:

$$Kcal = \frac{i \times Rvcm \times Kvcm}{i \times Rsense \times Ksense} \qquad \text{(Equation 1)}$$

if $Kvcm = 1$ and $Ksense = 1$ then

$$Kcal = \frac{i \times Rvcm}{i \times Rsense} \qquad \text{(Equation 2)}$$

At start-up, a small VCM current is applied towards the outer crash stop making V_{bemf} 340 = 0:

$$i \times Rvcm = Vvcm - Vref1, \; and \qquad \text{(Equation 3)}$$

$$i \times Rsense = Vrsense - Vref2 \qquad \text{(Equation 4)}$$

Therefore, the following relationship may be established:

$$i \times Rvcm = Kcal \times (i \times Rsense) \qquad \text{(Equation 5)}$$

Substitution yields the following equality:

$$(Vvcm - Vref1) = Kcal \times (Vrsense - Vref2) \qquad \text{(Equation 6)}$$

Thus, the microprocessor 390 may calibrate the control circuit 300 by determining the calibration gain coefficient Kcal as:

$$Kcal = \frac{Vvcm - Vref1}{Vrsense - Vref2} \qquad \text{(Equation 7)}$$

After calibrating the control circuit 300, the microprocessor 390 monitors V_{bemf} 340, at sample times, to determine whether to increase or decrease the current controlling the read/write head 160 velocity.

Figure 4 illustrates a calibration algorithm 400 that the control circuit 300 initiates to determine the gain calibration constant Kcal at power up. The calibration algorithm starts at step 410. At step 420, the current to the VCM coil is turned off. The microprocessor 390 reads the output of the ADC 380 through both the Vvcm 353 and V_{Rsense} 355 paths to determine the reference voltage corresponding to each path, step 425. A

small current is then applied to the VCM to move the read/write heads 160 in the unload direction, step 430 before the microprocessor 390 selects and reads the VCM voltage, Vvcm 353, step 440. The microprocessor 390 selects and reads the sense voltage, V_{Rsense} 355, step 450. In step 460, the microprocessor 390 calculates the calibration constant, Kcal, as:

$$Kcal = \frac{Vvcm - Vref1}{Vrsense - Vref2} \qquad \text{(Equation 8)}$$

The calibration algorithm 400 ends at step 470.

Figure 5 illustrates a load/unload algorithm 500 that the control circuitry 300 implements to control the velocity of the read/write heads 160 during a load/unload procedure, as illustrated in Figure 2. The algorithm starts at step 505. The microprocessor 390 determines whether the read/write heads 160 are being loaded or unloaded from the ramp, step 510. If the heads are being loaded from the ramp, the microprocessor sets the voltage corresponding to a target velocity of the read/write heads 160 as V_Load_Target, step 515. The microprocessor 390 then receives the Vvcm 353 and V_{Rsense} 355 voltages from the ADC 380, step 520. In step 525, the microprocessor 390 calculates the back emf voltage, V_{bemf} 340, as:

$$Vbemf = (Vvcm - Vref1) - Kcal \times (Vrsense - Vref2) \qquad \text{(Equation 9)}$$

In step 530, the microprocessor 390 uses the calculated value for V_{bemf} 340 to determine a velocity error as:

$$Verr = V\_Load\_Target - V_{bemf} \qquad \text{(Equation 10)}$$

In step 535, the microprocessor 390 performs a velocity compensation algorithm 600 as described below in Figure 6 to make adjustments to the read/write head velocity 160. The velocity compensation algorithm adjusts the transducer head velocity by comparing the voltage corresponding to the load target velocity with the voltage corresponding to the actual velocity of the transducer heads, as determined from V_{bemf} 340.

In step 540, the microprocessor 390 determines whether the read/write heads 160 have loaded on to the disk 120. If the loading procedure is not complete, the microprocessor 390 waits for one sample duration in step 547 before transferring control to step 520 to receive the Vvcm 353 and V_{Rsense} 355 voltages from the ADC 380. If the loading of the read/write head onto the disk is complete, the heads are locked into tracking mode, in step 545, before the load/unload algorithm 500 concludes at step 590.

In step 550, if the microprocessor 390 determines that the read/write heads 160 are being unloaded onto the ramp 210, the microprocessor 390 assigns the target velocity as V_Unload_Target. The microprocessor 390 then receives the Vvcm 353 and V_{Rsense} 355 voltages from the ADC 380 in step 555. In step 560, the microprocessor 390 may calculate V_{bemf} 340 according to equation 9:

$$Vbemf = (Vvcm - Vref1) - Kcal \times (Vrsense - Vref2) \qquad \text{(Equation 9)}$$

Using the calculated value for V_{bemf} 340, in step 565 the microprocessor 390 may determine the velocity error, Verr, as:

$$Verr = V\_Unload\_Target - V_{bemf} \qquad \text{(Equation 11)}$$

The microprocessor 390 then performs the velocity compensation algorithm 600 as described below in Figure 6 to make any necessary adjustments to the read/write head 160 velocity, step 570. The velocity compensation algorithm adjusts the velocity of the transducer heads by comparing the voltage corresponding to the load target velocity with the voltage corresponding to the actual velocity of the transducer heads, as determined from V_{bemf} 340.

The microprocessor 390 next determines whether the unloading of the read/write head has successfully completed, step 575. If the unloading procedure has not completed, the microprocessor 390 waits for one sampling period before transferring control to step 555 to receive the Vvcm

353 and V_{Rsense} 355 voltage measurements, step 580. If the unloading procedure has completed, the VCM is disabled, step 585. The load/unload algorithm 500 ends at step 590.

Figure 6 illustrates the velocity compensation algorithm 600 initiated by the microprocessor 390 to correct the velocity of the read/write heads 160. The velocity compensation algorithm begins at step 610. The microprocessor first determines the value of the velocity error, Verr(n), for the current sample period, step 620. This may be done, as previously described in steps 530 or 565 of the load/unload algorithm 500.

Next, the microprocessor determines the value of a discrete control variable, Control(n), that will be used by the driver circuit 310 to make adjustments to the head velocity. Although there are several methods of velocity compensation that are well known in the art and may be employed in the present invention, the preferred embodiment of the present invention employs the Proportional-Integral control technique, wherein Kp is a proportional constant and Ki an integral constant. Both Kp and Ki are selected according to the desired frequency and transient responses for the velocity control loop. The basic equation, in continuous time domain, for the velocity compensation algorithm 600 may be represented as:

$$Output\_command = \left(Kp + \frac{Ki}{S} \right) \times Verr \qquad \text{(Equation 12)}$$

Although a continuous time domain illustration is shown, the preferred embodiment of the present invention employs a microprocessor 390 that digitally processes the control signals. The above output control equation should therefore be implemented in the discrete time domain. In step 630, therefore, the microprocessor 390 calculates the value for the discrete control variable, Control(n), as:

$$Control(n) = Control(n-1) + Ki \times (T - Kp) \times Verr(n-1) + Kp \times (Verr(n)),$$

(Equation 13)

where (n) denotes the current sample and (n-1) denotes the previous sample.

The microprocessor 390 then sends the value for Control(n) to the driver circuit 310, where adjustments to the head velocity will be initiated, step 640. Using the current values for Control(n) and Verr(n), the microprocessor 390 sets the value of Control(n-1) and Verr(n-1) equal to the current values of Control(n) and Verr(n), so that these values may be used for velocity control during the next sample time, step 650. If the velocity compensationg algorithm 600 continues, control is transferred to step 620 wherein the microprocessor determines the value of the velocity error, Verr(n), for the current sample period. The velocity compensation algorithm 600 concludes at step 660.

EXAMPLE

By way of example, the following calculations represent an illustrative implementation of the present invention. Typical values for the VCM resistance and the sense resistors may be:

Rvcm 320 = 17.1 Ω

Rsense 330 = 1 Ω

Similarly, the gains of the first operational amplifier 350, Kvcm, and the second operational amplifier 360, Ksense may be:

Kvcm = 5

Ksense = 4

The preferred embodiment of the invention utilizes a 12-bit ADC converter 380 with a full-scale voltage of 5 volts. Thus, the resolution of the preferred ADC converter 380 may be:

$$ADC\_resolution = \frac{ADC\_FS\_voltage}{2^{ADC\_bits} - 1} = \frac{5}{2^{12} - 1} = 1.221.10^{-3} \quad \text{V/count}$$

(Equation 14)

The reference voltage, Vref 357, when V_{bemf} 340 = 0, may be 2.5 volts. Because different offset voltages may exist for the paths of Vvcm and V_{Rsense}, the reference voltage through each path may not be identical to Vref 357. If Vref1 and Vref2 are defined as the reference voltages at the ADC 380 for each respective path, these voltages may be:

$$Vref1 = 2.520 \text{ volts; and}$$

$$Vref2 = 2.510 \text{ volts.}$$

Thus, the ADC 380 count corresponding to the reference voltage for each path would be:

$$ADC\_Vref1\_count = \frac{Vref1.2^{ADC\_bits}}{ADC\_FS\_voltage} = 2064$$

$$ADC\_Vref2\_count = \frac{Vref2.2^{ADC\_bits}}{ADC\_FS\_voltage} = 2056$$

Setting I_{vcm} to 10 mA may then yield a value for Vvcm 353 of:

$$Vvcm.353 = Vref1 + Ivcm \times Rvcm.320 \times Kvcm$$

$$= 2.52 \text{ v} + 10 \text{ mA} * 17.1\ \Omega\ * 5$$

$$= 3.375 \text{ volts}$$

The ADC converter 380 count corresponding to this Vvcm voltage 353 is:

$$ADC\_Vvcm\_count = Integer\left(\frac{Vvcm.2^{ADC\_bits}}{ADC\_FS\_voltage} - ADC\_Vref1\_count\right)$$

(Equation 15)

$$= (3.375 \text{ v} * 4096) / 5\text{v} - 2064$$

$$= 701$$

Similarly, the ADC converter 380 count corresponding to the V_{Rsense} 355 may be calculated by first determining the value of V_{Rsense} 355 as:

$$Vrsense = Vref2 + Ivcm \times Rsense \times Ksense \qquad \text{(Equation 16)}$$

$$= 2.51 + 10 \text{ mA} * 1\ \Omega * 4$$

$$= 2.55 \text{ volts}$$

This value of V_{Rsense} 355 corresponds to the following ADC 380 count:

$$ADC\_Vrsense\_count = Integer\left(\frac{Vrsense.2^{ADC\_bits}}{ADC\_FS\_voltage} - ADC\_Vref2\_count\right)$$

(Equation 17)

$$= (2.55\ v * 4096) / 5v - 2056 = 33$$

Finally, the value for the calibration gain, Kcal, for the preferred embodiment is determined as:

$$Kcal = \frac{ADC\_Vvcm\_count}{ADC\_Vrsense\_count} \qquad \text{(Equation 18)}$$

$$= 700 / 33 = 21.21$$

It should be understood that the number of bits in the ADC 380 may be increased if greater accuracy or resolution is desired, or the number of bits in the ADC 380 may be reduced to decrease computational burden.

It will be apparent to those skilled in the art that various modifications and variations can be made to the hard disk drive ramp load/unload methodology without departing from the spirit or the scope of the invention. Thus, it is intended that the present invention covers the modifications and variations of this invention provided that they come within the scope of any claims and their equivalents.